A Low Power, Wide Dynamic Range Multi-Gain Signal Processor for the SNAP CCD.

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***Abstract*-- A four-channel custom chip designed for reading out the CCDs of the SNAP satellite visible imager is presented. Each channel consists of a single-ended to differential converter followed by a correlated double sampler and a novel multi slope integrator. The output signal is differentially brought out of the chip by an output buffer. This circuit is designed to operate at room temperature for test purpose and at 140K, which will be the operating temperature. The readout speed is 100kHz. The 16-bit dynamic range is covered using 3 gains each with a 12 bit signal to noise ratio. The prototype chip, implemented in a 0.25µm CMOS technology, has a measured readout noise of 7µV rms at 100kHz readout speed, a measured non-linearity of ±0.025% and a power consumption of 6.5mW.**

I. Introduction

A four-channel custom chip designed for reading out charge coupled devices (CCD) is presented. This design is part of the research and development program for the SNAP (Super Nova/-Acceleration Probe) project. SNAP is an international satellite proposal dedicated to understanding the dark energy responsible for the accelerating expansion of our universe. It has a 2 meter telescope with a large field of view. CCDs and near infrared detectors are located on the focal plane for imaging and spectroscopy. The primary goal of this circuit is to cover a 16-bit dynamic range with a readout noise of 7µV rms (2 electrons) referred to the input at 100kpixel/s readout speed. The operating temperature of 140K is needed to lower the detector dark current.

The circuit described is intended to operate close to the CCDs in order to avoid long cable connections and minimize pick-up noise. This gives additional constraints to the circuit such as low power consumption, operation at 140K and radiation tolerance to a total dose of 10krad. This paper is organized as follows. In section II, the signal processing method used in this design is described. The circuit architecture and the principle of operation are presented in Section III. Detailed descriptions of some critical blocks are presented in Section IV. Section V is devoted to simulation results and chip layout is discussed in section VI. Experimental results are presented in section VII.

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II. Signal Processing Method

The output signal from a CCD needs to be processed to remove the reset level, reduce the noise and accommodate the dynamic range before being digitized.

A. Noise Study

Several types of signal processing methods suitable for optimizing the signal over noise ratio of a CCD are reviewed in [1]. SNAP plans to use the LBNL high resistivity, p-channel CCD. This device has a noise spectral density at the output stage with a thermal noise component of $20nV/Hz^{1/2}$ and a 1/f noise of $1.5\mu V/Hz^{1/2}$ at 1 Hz with a frequency exponent of 1. According to [1], the most appropriate technique is the differential averager which consists of a correlated double sampler (CDS) followed by an integrator, as the thermal noise level of the CCD is high. This technique was simulated by injecting modeled noise spectral densities of the dominant noise sources into a behavioral model. These are the CCD source follower output stage and the front-end circuit input stage. The block diagram of this model is shown in Fig. 1. The first stage converts the single-ended input signal to a differential signal with a voltage gain of 4, using two ideal operational amplifiers labeled A1 and A2 with resistive feedback. A switch matrix is used to implement the correlated double sampling function. The last stage is an ideal differential integrator. The spectral noise density labeled Vn of the amplifiers A1, A2 and A3 has a thermal noise level of $4nv/Hz^{1/2}$ and a 1/f noise of $1\mu V/Hz^{1/2}$ at 1Hz with a frequency exponent of 1. This spectral density is a model of an input differential pair biased with a tail current of 200µA and an aspect ratio of 1000. The CCD noise source is also injected at the input with the spectral density described above. Transient noise analysis was performed using the Eldo simulator tool [2], with an integration time $T=2\tau$ of 8µs. The CCD noise contribution is 10µV rms, while the front-end noise contribution is 6.3µV rms, both referred to the input. Hence the total noise referred to the input noise is 12µV, which is the square root of the quadratic sum of the CCD noise and the front-end noise.

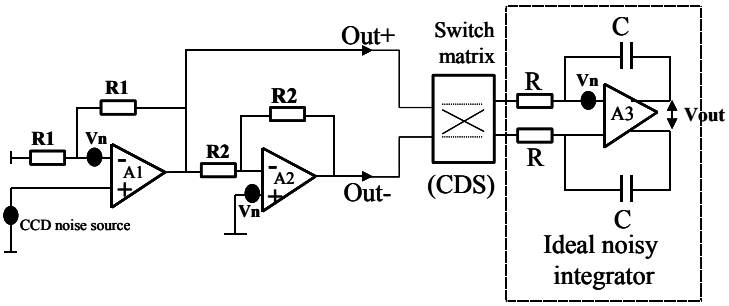

Fig.1: Behavioral model used to simulate the noise contribution of the CCD and front-end circuit filtered by a differential averager.

These results are in a good agreement with the equations developed in [1]. The conversion gain of the CCD is 3.5µV/e. The noise requirement for the focal plane is 4 electrons rms for a readout frequency of 100kHz. The simulation results give a total noise of 12µV/3.5µV/e=3.4e rms which meets the requirements with some margin.

B. Dynamic Range

The dynamic range requirement is 16-bit, from 2 electrons to 130k electrons. However, the requirement for the S/N is driven by the Poisson process of the light interacting in the sensor which has a variance equal to N, where N is the number of incoming photons [3]. The signal can be digitized with an LSB size that depends on the signal amplitude such that the ADC quantization noise is still below the Poisson noise. This concept has been implemented on chip using a novel 3-slope multi-range integrator with voltage gains of 32, 2 and 1 for a given integration time. In this case a 12-bit resolution ADC is sufficient, and the quantization noise referred to the input is 1 electron for an integrator gain of 32. Fig. 2 shows the contributions of the Poisson process, the electronic noise and the quantization noise to the resolution dN/N referred to the input, as a function of the signal amplitude N. The resolution dN/N due to the Poisson process and the electronic noise is given by

$$\frac{dN}{N} = \sqrt{\left(\left(\frac{N_{el}}{N}\right)^2 + \left(\frac{1}{N}\right)^2\right)} \qquad (1)$$

where, N_{el}=1.8 e rms is the front-end noise.

The resolution dN/N due to the quantization noise is given by

$$\frac{dN}{N} = \frac{N_{fs}}{NG2^n} \qquad (2)$$

Where N_{fs} is the full scale signal, G is the integrator gain and n the number of bits.

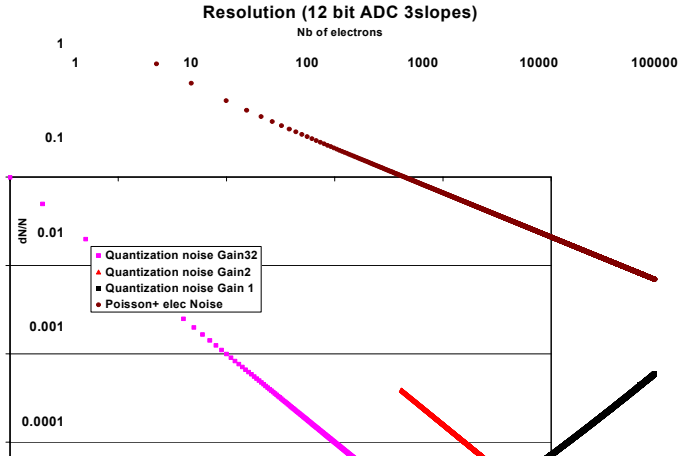

Fig. 2: Resolution dN/N referred to the input as a function of the input signal N for the Poisson process, the quantization and electronic noise contribution. A 12-Bit resolution ADC and an integrator gain of 32, 2 and 1 are assumed in this case.

III. Channel Architecture

The differential averager technique depicted in Fig. 1 along with a novel 3-slope multi-range integrator accommodating the 16-bit dynamic range with a 12-bit resolution was implemented on a chip. The block diagram of one channel is shown in Fig 3 and the associated timing diagram is shown in Fig 4.

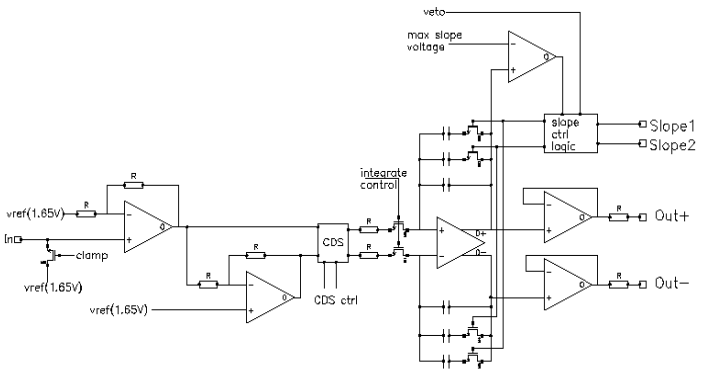

Fig. 3: Channel block diagram.

The channel consists of a single-to-differential converter followed by a correlated double sampler (CDS) and a multi-range gated integrator. The output signal is differentially brought out of the chip by two output buffers. The CCD is AC-coupled to the input of the channel. A clamp switch, controlled by the signal labeled “clamp”, restores the input baseline to a fixed potential V_{ref} during the CCD reset phase. The CDS subtracts the low frequency noise, the CCD pixel reset level, and the offset from the single-to-differential stage.

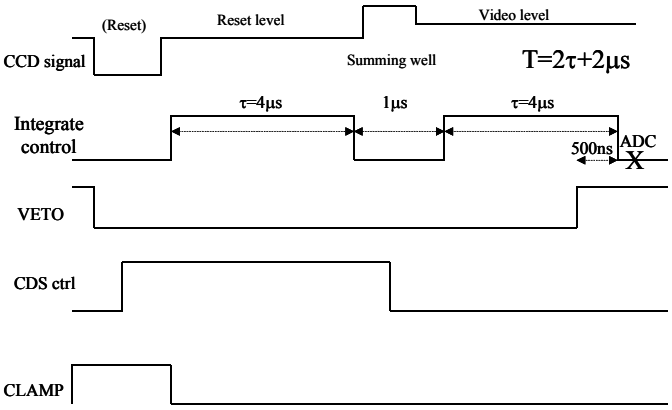

Fig. 4:Timing diagram

The multi-range integrator consists of a fully differential OTA fed back by an RC network setting the integrator gain. Depending on the capacitance value, the integrator has a gain of 32, 2 or 1. A pair of first-order charge injection compensated switches in series with the resistance control the integration time. The multi-range operation is as follows. After resetting the integrator (reset switches not shown on the figure), the integrator switch, controlled by the signal labeled "integrate control", is turned on and the CCD reset level is integrated for 4μs. During the next 1μs, the switch is turned off and the integrator is insulated from the CDS operation (controlled by the signal labeled "CDS ctrl") and input signal transient, without disturbing the charge already stored in the feedback capacitors. Once the input signal is settled, the integration starts again for 4μs. At the beginning the default gain setting is 32. A logic circuitry automatically switches to the gain 2 and 1 if the output signal exceeds a threshold. This threshold is set to 80% of the full scale. The logic provides two signals labeled slope1 and slope2 indicating the integrator gain at the end of the processing cycle. Besides the automatic gain change mode, each gain can be forced individually. A signal labeled "veto" disables the logic circuitry 500ns before the end of the signal integration time, to avoid any gain changes just before stopping the integration. The data is ready to be digitized a couple of hundred ns after the end of the signal integration time (position labeled ADC in Fig.4). Two buffers are connected to the positive and negative outputs of the integrator to drive off-chip circuitry.

IV. Circuit Description

This section focuses on more detailed circuit descriptions of the sensitive parts of the design linked to the circuit performance needed. This concerns particularly the multi-range integrator.

A. Single-to Differential Converter and Correlated Double Sampler

The full-scale input signal is typically +500mV. The single-to-differential stage has a gain of 4 in order to reduce the noise contribution of the integrator. A 500mV full-scale signal generates a 2V differential signal, at the input of the CDS, with a common mode component at Vdd/2. The amplifiers have large DC gain (120 dB) in order to achieve good linearity when the signal is settled (reset and signal plateau). The settling time is about 200ns to achieve 16 bits linearity. The opamp employed in this design has a conventional folded input stage [4] followed by a Miller-compensated class A/B stage [5]. An enhanced slew rate source follower [6] is used as the opamp output stage in order to drive the resistive feedback network. The opamp input differential pair is biased with a tail current of 200μA, achieving a thermal noise spectral density of about $4nV/Hz^{1/2}$ and has an aspect ratio of a 1000.

The CDS has a four-switch matrix. The on resistance of these switches depends on the signal amplitude as they are in series with the integrator resistor. Care has been taken to size them such that their on resistance variation over the full signal range is a small fraction of the total integrator resistance value (<0.02%) to keep the linearity.

B. Multi Range Integrator

The multi-slope integrator schematic is depicted in Fig. 5. A bank of capacitors in the feedback along with the resistor R1 set the integrator gain to 32, 2 or 1 depending on the S1 and S2 switch settings. The resistance R1 is 50kΩ and the total capacitance in the feedback is 2.5pF, 40pF or 80pF. The amplifier labeled A is a conventional fully differential single-stage folded cascode OTA [7]. The degenerated differential input pair is biased with a tail current of 400μA.

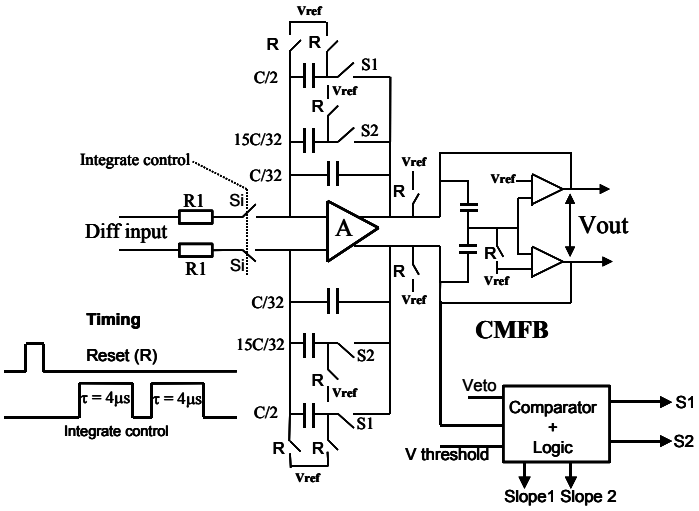

Fig. 5: Multi-slope integrator.

A dynamic switched capacitor common-mode feedback circuit (CMFB) senses and sets the common-mode voltage at the integrator output [8]. During the reset period, the switches labeled R set the common mode voltage to V_{ref} (Vdd/2) at both the input and output and discharge the feedback capacitors. Once the reset switches R are turned off, the common-mode feedback circuit controls the common voltage at the output. The switches S_i start and stop the signal integration. A single stage comparator followed by a Schmitt trigger senses and compares the output signal to $V_{threshold}$. If it exceeds the

threshold voltage, the switch S2 is turned on first, changing the gain from 32 to 2. If the output signal is again above threshold, the switch S1 is turned on and the gain becomes 1.

During the switching time, a charge error is introduced because the OTA virtual ground moves. This error is constant as we are switching from one slope to another with the same output signal amplitude. The integrator output voltage is digitized when the integration is done and then the OTA virtual ground is equal to the output voltage divided by the DC gain (hold mode).

V. Simulation Results

The circuit was extensively simulated using the Eldo simulator tool. Typical and corners model parameters were used for simulation at both 300K and 140K. At 140K, the threshold voltage of transistors is increased by 160mV for both N and P type. The carrier mobility also increases by a factor of 1.7 for both NMOS and PMOS compared to room temperature. This effect can have an impact on the linearity and stability of the active parts and has been taken into account. Model parameters were adjusted according to measurements we have performed on test transistors.

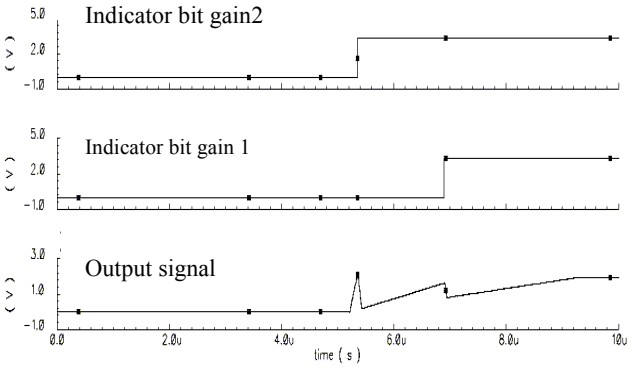

Fig. 6: Slope indicator bits and analog output signal of the channel for a full scale input signal of 500mV. The readout cycle is 10µs.

Fig. 6 shows the simulated output signal of the channel for a full-scale input voltage of 500mV. The readout cycle is 10µs. The two upper traces are the slope indicator bits, indicating two gain changes as expected. The bottom trace shows the integrator output through the output buffer. Fig. 7 shows the simulated deviation from the best-fit line of the channel as a function of the input signal over the 3 ranges. A simulated non-linearity of ±1 LSB (12-Bit) is obtained at both 300K and 140K.

Noise simulations in the time domain using the transient noise analysis of the Eldo simulator were performed on the channel. The input referred noise level is 7µV rms at 300K and 5.6µV at 140K. As the CCD conversion gain is 3.5µV/electron, the corresponding input referred noise in electrons is 2 and 1.6, respectively.

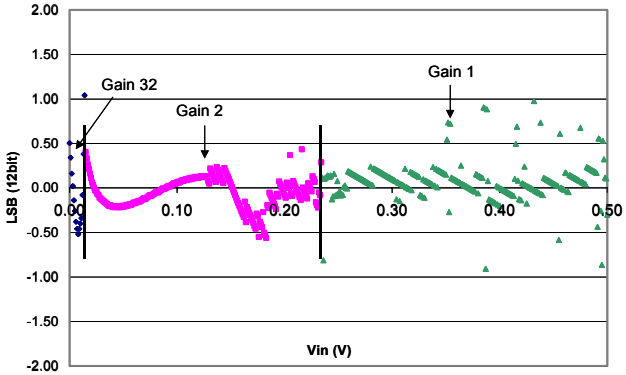

Fig. 7: Simulated non-linearity of the channel as a function of the input signal, over the 3 ranges. The readout cycle is 10µs. The saw-tooth structure is an artifact of the simulator numerical precision.

VI. Chip Layout

The prototype chip is implemented in a commercial 0.25µm mixed-mode CMOS technology. The die size is 3.6mm x 5.4mm. A photo of the die is shown in Fig. 8. The chip contains 4 channels along with stand-alone building blocks such as the single-to-differential converter and the multi-range integrator for test purposes.

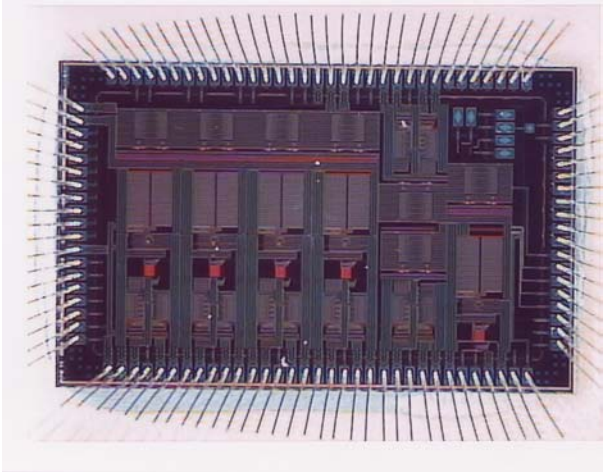

Fig. 8: Photograph of the prototype chip.

VII. Experimental Results.

The prototype chip is packaged in a 120-pin CERQUAD package and has been tested using a 16-bit resolution test board, including DACs to inject signal at the input and ADCs to digitize the signal at the output. A pattern generator provides LVDS control signal to the chip. The operation of the circuit is verified with a supply voltage range from 3.1V to 3.3V. All results given are obtained with a 3.3V supply unless otherwise specified. The reference voltage V_{ref} needed to set the common voltage of the channel is set to 1.65V (Vdd/2). The performance of the chip is measured at room temperature and at 140K by using a tailored test board in a liquid nitrogen cooled dewar.

A. Non-Linearity Measurement

Fig. 9 shows the integrator output for a large signal applied at the input (upper trace) along with the two gains change indicator bits (lower traces). A linearity measurement has been performed by injecting an input signal generated by the DAC ranging from 0 to full-scale at a read rate of 100KHz. The deviation from the data and a best-fit line has been extracted over the three gains and is shown in Fig. 10.

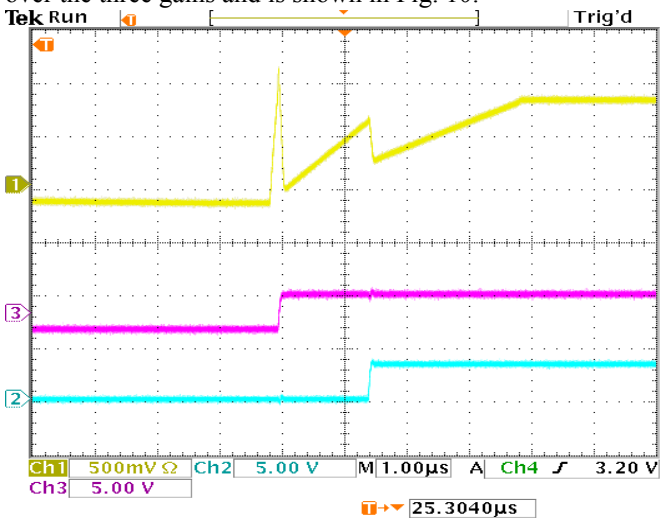

Fig. 9: Channel output signal and gain change indicator bits for a large input signal. The readout cycle is 10µs. ADC conversion occurs at the far right of the top trace.

The measured non-linearity is ±1LSB (12-bit) at 300K and ±0.6 LSB at 140K. With a 3.1V supply at 140K, the measured non-linearity is ±1.25LSB.

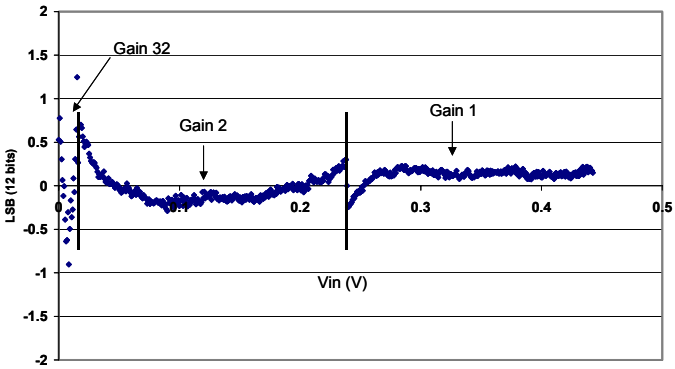

Fig. 10: Measured non-linearity as a function of the input signal at 300K.

B. Noise Measurement

A set of noise measurements at both temperatures was done by histograming the output voltage and calibrating the channel to get the exact conversion gain. A noise of 7µV rms (2 electrons) referred to the input was measured at 100kpixel/s readout rate and 300K. At 140K, the measured noise decreases by 20% with an rms value of 5.6µV (1.6 electrons) as expected.

C. Measurements Summary

A summary of the achieved channel performances at 300K and 140K is shown in Table 1 and Table 2 respectively. The measured power consumption is 6.6mW.

Table 1: Summary of the channel performances at 300K.

Parameter	Value
Dynamic range	16-bit
Noise (100KHz readout rate)	7µV rms (2e)
Noise (50KHz readout rate)	5.25µV rms (1.5e)
Non-linearity	±1LSB (12-bit)
PSRR	74 dB (100KHz)
Gain temperature coefficient	400ppm/K

Table 2: Summary of the channel performances at 140K.

Parameter	Value
Noise (100KHz readout rate)	5.6µV rms (1.6e)
Noise (50KHz readout rate)	4.65µV rms (1.33e)
Non-linearity	±0.6LSB (12-bit)
PSRR	74 dB (100KHz)
Gain temperature coefficient	400ppm/K

VIII. Conclusion

A 16-bit linear multi-gain signal processor for the SNAP CCD has been achieved using a novel 3-range integrator each with a 12-bit signal to noise ratio. Crucial parameters such as power consumption, noise, linearity and operation at 140K were studied to obtain a reliable design. Experimental tests were performed to assess the performance of the circuit. We are now integrating the circuit with a CCD for a system test at 140K to verify the signal processing efficiency with respect to the noise.

IX. References

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